AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows:

Please amend paragraphs [047], [090], [093], and [095] as follows:

[047] As discussed above, the product of the factors of the numerator, $(A_1)*(A_2)*(A_3)*\cdots*(A_M)$, is computed by scaling each factor in a group by a corresponding scale factor. Control module ~~13~~ 110 uses running sum unit 130 to compute a running sum of the scale factors. If the floating point operand, F, corresponds to the operand to be scaled by the scaling unit 120, the integer K, represents the amount by which the operand is scaled by scaling unit 120. Accordingly, as scaling unit 120, through a series of iterations, scales the factors in a group, running sum unit 130 may generate a running sum that corresponds to the sum of the scale factors used by scaling unit 120 as follows. During the first iteration of the first group of factors of the numerator, operand J of running sum unit 130 equals zero and a first factor of the group is input as operand F. Running sum unit 12 determines an integer, K, such that the value, $F*2^{-K}$, is greater than or equal to one and less than two and adds the integer K to operand J. For each subsequent iteration, the result of the previous iteration is input as operand J and the next factor of the group is input as operand F. These iterations continue until the last factor in the group is processed.

[090] The result generator 330a may be in the form of a floating point multiplier unit 74 as disclosed in U.S. Patent Application Serial No. 10/035,580, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point Multiplier With Embedded Status Information," assigned to the assignee of the present application. The result is coupled to result bus 75.

[093] The scaling unit 120b is identical to the scaling unit 120a described above, except that scaling unit 120b includes a count trailing zeros circuit ~~161~~ 192, a "binary to 1-of-23" circuit 194, and twenty-three gates 195, instead of a normalizer 92. Since, except for the delimiter flag, the fraction field of an operand in the delimited format is normalized, the scaling unit 120b may clear only the delimiter flag. Therefore, instead of a normalizer 92, the scaling unit 120b includes the count trailing zeros circuit ~~161~~ 192, the "binary to 1-of-23" circuit 194, and the twenty three gates 195 to clear the delimiter flag. The count trailing zeros circuit 192 generates output signals representing the number n, where n equals the number of bits equal to zero to the right of the delimiter flag. The "binary to 1-of-23" circuit 194 generates twenty three bits equal to zero, except the bit in the bit position n+1 from the right, corresponding the bit position of the delimiter flag in the fraction field bits of the operand in operand buffer 300B. The twenty three gates 195 operate to pass all the fraction field bits of the operand to the multiplexer ~~193~~ 93, except the delimiter flag, which is set equal to zero. Otherwise, the scaling unit 120b ~~running sum unit 130b~~ operates in the same manner scaling unit 120a ~~as running sum unit 130a~~ and includes floating-point multiplier 174.

[095] The scaling units 130c and 130d are generally similar to scaling units 130a and 130b, respectively, except that comparators 81, 83, 85, and 86 and logic element 88 have been removed in the operand analysis circuits 310c and 310d because there is no underflow 1320 and overflow 1350 format in IEEE Std. 754 and no status flag information stored in the operand in IEEE Std. 754. Further, because no status flag information is stored in the operand in IEEE Std. 754, the result generator 330c including floating-point multiplier 274 may correspond to a multiplier unit for performing conventional multiplication operations in accordance with IEEE

Std. 754. The result generator 330d including floating point multiplier 374 may correspond to a multiplier unit as disclosed in U.S. Patent No. 6,131,106.